

Our Docket No.: 51876P549  
Express Mail No.: EV 339916502US

UTILITY APPLICATION FOR UNITED STATES PATENT  
FOR  
SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR GENERATION OF CORE VOLTAGE

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# SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR GENERATION OF CORE VOLTAGE

## Field of Invention

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The present invention relates to a semiconductor memory device; and, more particularly, to a semiconductor memory device and a core voltage generating method for stabilization of the core voltage during a refresh operation of the semiconductor memory device.

## Description of Prior Art

Generally, a semiconductor memory device is supplied with an external voltage VDD, and lowers a voltage level of the external voltage VDD to voltage levels of a core voltage V<sub>CORE</sub> and a peri voltage V<sub>PERI</sub> for operation of the semiconductor memory device; herein, the core voltage V<sub>CORE</sub> is used for reading data from a memory cell or writing data to the memory cell, and the peri voltage V<sub>PERI</sub> is used for operating internal circuits included in the semiconductor memory device.

Typically, in a conventional semiconductor memory device, a voltage level of the core voltage V<sub>CORE</sub> becomes unstable because excessive power consumption is occurred when a bit line is charged.

A core voltage generator raises the unstable core

voltage V<sub>CORE</sub> to a stable voltage level. The core voltage generator determines whether or not the core voltage V<sub>CORE</sub> is stable by comparing the core voltage V<sub>CORE</sub> with a reference voltage V<sub>RC</sub>.

5        Herein, when the core voltage V<sub>CORE</sub> is unstable, an over driving controller is activated to drive the external voltage V<sub>DD</sub> over the core voltage V<sub>CORE</sub>.

10        R<sub>TOE</sub> and S<sub>BE</sub> are signals for the bit line charging. The conventional semiconductor memory device slows down activating speed of the R<sub>TOE</sub> and S<sub>BE</sub> to slow down power consuming speed of the core voltage V<sub>CORE</sub> during the bit line charging.

15        That is, the R<sub>TOE</sub> and S<sub>BE</sub> are activated to a logic 'LOW' level and to a logic 'HIGH' level respectively, and a predetermined time is needed to change levels of the R<sub>TOE</sub> and S<sub>BE</sub>. The semiconductor memory device extends the predetermined time so that the R<sub>TOE</sub> and S<sub>BE</sub> are activated slowly. Therefore, a voltage level of the core voltage V<sub>CORE</sub> is slowly downed.

20        Fig. 1 is a block diagram showing a power supply unit included in the conventional semiconductor memory device.

As shown, the conventional semiconductor memory device includes an over driving controller 11, a core voltage generator 10, a bit line sensing amplifier 12 and a bit line sensing amplifier controller 13.

25        The over driving controller 11 receives a bit line sensing start signal SE<sub>ST30</sub> and generates an over driving control signal SENSE\_EN for driving an external voltage V<sub>DD</sub>

over a core voltage V<sub>CORE</sub>. The core voltage generator 10 generates the core voltage V<sub>CORE</sub> for operating the bit line sensing amplifier 12 in response to the bit line sensing start signal SE<sub>ST30</sub> and the over driving control signal SENSE\_EN.

5       The bit line sensing amplifier 12 amplifies a potential difference between a bit line pair BL and BLB. The bit line sensing amplifier controller 13 generates a first enable signal RTOE and a second enable signal SBE. Herein, the first enable signal RTOE and the second enable signal SBE are for  
10   enabling a first activating voltage RTO (not shown) and a second activating voltage SB (not shown) each, where the first activating voltage RTO and the second activating voltage SB are for operating the bit line sensing amplifier 12.

Fig. 2 is a circuit diagram showing the core voltage  
15   generator 10 shown in Fig. 1.

As shown, the core voltage generator 10 includes a control unit 101, a comparing unit 102, a core voltage comparing operator 103 and an over driving unit 104.

The control unit 101 turns on or off the comparing unit  
20   102 depending on the bit line sensing start signal SE<sub>ST30</sub>. The comparing unit 102 compares the reference voltage V<sub>RC</sub> with the core voltage V<sub>CORE</sub> to generate an enable signal COMP\_EN depending on the comparison result. The over driving unit 104 generates the core voltage V<sub>CORE</sub> in response to the over  
25   driving control signal SENSE\_EN.

The control unit 101 has an inverter I3, a PMOS transistor P1 and NMOS transistors N4 and N5.

Herein, the inverter I3 inverts the bit line sensing start signal SEST30. An output of the inverter I3 is connected to a gate of the PMOS transistor P1 and a source of the P1 is connected to an external voltage VDD. A gate of the NMOS transistor N4 is connected to the output of the inverter I3, a drain of the N4 is connected to a drain of the P1, a source of the N4 is connected to a ground voltage VSS. A drain and a gate of the NMOS transistor N5 are connected to the drain of the P1, a source of the N5 is connected to the ground voltage VSS.

The comparing unit 102 has PMOS transistors P2, P3, P4 and P5; and also has NMOS transistors N1, N2, N3, N6, N7, N8 and N9.

Herein, the P2 is paired with the P3 constituting a differential amplifying unit, and the P4 is paired with the P5 also constituting the differential amplifying unit. The N2 is controlled by the reference voltage VRC, and the N3 is controlled by the core voltage VCORE. The N2 and N3 are input units for the differential amplifying unit. The N7 serves as a current source for the differential amplifying unit. A gate of the N1 is connected to the reference voltage VRC and a source of the N1 is connected to a power voltage VDD. A gate of the N6 is connected to the gate of the N5. The N6 is connected between the drain of the N1 and the ground voltage VSS. A gate of the N8 is connected to the gate of the N7, and connected between the drain of the N9 and the ground voltage VSS.

Herein, the gate of the N3 is connected to the drain of the N9, and the gate of the N2 is connected to the drain of the N1.

A gate of the P6 included in the core voltage comparing operator 103 receives an enable signal COMP\_EN. A source of the P6 is connected to the power voltage VDD and a drain of the P6 is connected to a gate of the N9.

A gate of the P7 included in the over driving unit 104 receives the sense enable signal SENSE\_EN. A source of the P7 is connected to the power voltage VDD and a drain of the P7 is connected to the gate of the N9.

Figs. 3A and 3B are circuit diagrams showing two different embodiments of the over driving controller 11. A first embodiment shown in Fig. 3A is provided with a plurality of inverters. Meanwhile, a second embodiment shown in Fig. 3B is provided with a plurality of PMOS capacitors.

As described above, the over driving controller 11 generates the over driving control signal SENSE\_EN for driving the power voltage VDD over the core voltage VCore after the conventional semiconductor memory device is activated.

Referring to Fig. 3A, the over driving controller 11 includes inverters I31 to I37 and a NAND gate NAND31.

The inverters I31 to I37 invert and delay a bit line sensing start signal SESt30. The NAND gate NAND31 receives the bit line sensing start signal SESt30 and an outputted signal from the inverters I31 to I37, and performs NAND operation on the two received signals, i.e., the bit line

sensing start signal SEST30 and the outputted signal from the inverters I31 to I37.

Referring to Fig. 3B, the over driving controller 11 further includes inverters I38 to I43, a NAND gate NAND32, an NMOS transistor N31 and PMOS transistors P31 to P38.

Figs. 4A and 4B are circuit diagrams showing the bit line sensing amplifier 12.

Fig. 4A shows a power supplying unit of the bit line sensing amplifier 12, and Fig. 4B shows an amplifying unit of the bit line sensing amplifier 12.

Referring to Fig. 4A, the power supplying unit of the bit line sensing amplifier 12 includes a first supplying unit 40 and a second supplying unit 41.

Herein, a first activating voltage RTO is supplied power by the core voltage VCORE or the power voltage VDD in response to first enable signal RTOE. A second activating voltage SB is supplied power by the ground voltage VSS in response to a second enable signal SBE.

The first supplying unit 40 is formed by a PMOS transistor P41; herein, a gate of the P41 is connected to the first enable signal RTOE, a source of the P41 is connected to the core voltage VCORE and outputs the first activating voltage RTO from a drain of the P41.

The second supplying unit 41 is formed by an NMOS transistor N41; herein, a gate of the N41 is connected to the second enable signal SBE, a source of the N41 is connected to the ground voltage VSS and outputs the second activating

voltage SB from a drain of the N41.

Referring to Fig. 4B, the amplifying unit of the bit line sensing amplifier 12 includes cross-coupled four transistors N51, N52, P51 and P52.

5 Fig. 5 is a circuit diagram showing the bit line sensing amplifier controller 13 shown in Fig. 1.

As described above, the bit line sensing amplifier controller 13 receives the bit line sensing start signal SEST30 and the refresh signal REFB, and generates the first enable signal RTOE and the second enable signal SBE for enabling the first activating voltage RTO and the second activating voltage SB shown in Figs 4A and 4B.

As shown, the bit line sensing amplifier controller 13 is provided with inverters I51 to I54, PMOS transistors P51 to P54, NMOS transistors N51 to N54 and resistors R51 and R52.

The I51 and I52 are connected serially and delay the bit line sensing start signal SEST30 for a predetermined time. The delayed bit line sensing start signal SEST30 is inputted to a gate of the P51, and the P51 outputs the first enable signal RTOE through its drain.

A gate of the N51 is connected to the gate of the P51 and controlled by the bit line sensing start signal SEST30. Drains of the N52 and N53 are connected to a source of the N51 and their gates are connected to the power voltage VDD and the refresh signal REFB respectively.

The resistor R51 is serially connected to the N52 and the ground voltage. The I53 is for inverting the bit line



sensing start signal SEST30.

The inverted bit line sensing start signal SEST30 is inputted to a gate of the P54 and controls the P54. The P54 outputs the second enable signal SBE from its drain. The N54  
5 is controlled by the bit line sensing start signal SEST30 and its gate and source are connected to the gate of the P4 and the ground voltage VSS respectively.

One end of the resistor R52 is connected to the power voltage VDD, and the other end of the R52 is connected to the  
10 P52 and P53. The I54 inverts the refresh signal REFB. Gates of the P52 and P53 are connected to the power voltage VDD and the inverted refresh signal REFB respectively.

Referring to Figs. 1 to 5, an operation of the power supply unit included in the conventional semiconductor memory  
15 device is described below.

If the power supply unit is activated, the bit line sensing start signal SEST30 becomes a logic 'HIGH' level, and the core voltage generator 10, the over driving controller 11 and the bit line sensing amplifier are enabled or start to  
20 operate.

If the bit line sensing start signal SEST30 becomes a logic 'HIGH' level, the core voltage generator 10 enables the comparing unit 102 for comparing the reference voltage VRC with the core voltage VCORE.

25 Herein, if the core voltage VCORE becomes lower than the reference voltage VRC, the enable signal COMP\_EN becomes a logic 'LOW' level and the PMOS transistor P6 is turned on

driving the power voltage VDD over the core voltage VCORE. If the core voltage VCORE is higher than the reference voltage VRC, the COMP\_EN becomes a logic 'HIGH' level and the PMOS transistor P6 is turned off separating the power voltage VDD from the core voltage VCORE.

The PMOS transistor P7 included in the over driving unit 104 controlled by the over driving control signal SENSE\_EN to drive the power voltage VDD over the core voltage VCORE.

The over driving controller 11 generates the over driving control signal SENSE\_EN if the bit line sensing start signal SEST30 becomes a logic 'HIGH' level. As described above, the over driving controller 11 can be embodied like a circuit shown in Fig. 3A or a circuit shown in Fig. 3B.

If the bit line sensing amplifier 12 is activated, the first enable signal RTOE generated from the bit line sensing amplifier 13 is enabled to turn on the PMOS transistor P41, and the first activating voltage RTO for operating the bit line sensing amplifier 12 is supplied with the core voltage VCORE.

At the same time, the second enable signal SBE is enabled to turn on the NMOS transistor N41, and the second activating voltage SB for operating the bit line sensing amplifier 12 is supplied power by the ground voltage VSS.

Therefore, the bit line sensing amplifier 12 consumes the first activating voltage RTO supplied with the core voltage VCORE for bit line charging. In the bit line sensing amplifier controller 13 shown in Fig. 5, if the bit line

sensing start signal SEST30 becomes a logic 'HIGH' level, the first enable signal RTOE becomes a logic 'LOW' level and the second enable signal SBE becomes a logic 'HIGH' level.

Meanwhile, in the bit line sensing amplifier controller  
5 13, the resistors R51 and R52 are included for controlling activating speed of the first enable signal RTOE and the second enable signal SBE so that the RTOE and the SBE can be activated slowly.

Therefore, the core voltage V<sub>CORE</sub> is merely lost during  
10 the refresh operation.

Figs. 6 and 7 are timing diagrams showing variations of the core voltage V<sub>CORE</sub> during the normal operation shown in Fig. 6 and the refresh operation shown in Fig. 7 of the conventional semiconductor memory device.

15 As shown in Fig. 6, at the normal operation, the timing of driving the power voltage V<sub>DD</sub> over the core voltage V<sub>CORE</sub> is same as the timing of consuming the core voltage V<sub>CORE</sub>.

However, as shown in Fig. 7, at the refresh operation, the timing of driving the power voltage V<sub>DD</sub> over the core  
20 voltage V<sub>CORE</sub> is different from the timing of consuming the core voltage V<sub>CORE</sub>, whereby the core voltage V<sub>CORE</sub> rises excessively.

#### Summary of Invention

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It is, therefore, an object of the present invention is to provide a semiconductor memory device for stabilizing a

core voltage during a refresh operation.

In accordance with an aspect of the present invention, there is provided a core voltage control device including a bit line sensing start signal controller for receiving a bit line sensing start signal to generate a delayed bit line sensing start control signal in response to a refresh signal; a core overdriving controller for generating an overdriving control signal in response to the delayed bit line sensing start signal; and a core voltage generator for generating the core voltage in response to the delayed bit line sensing start signal and the overdriving control signal to thereby provide core voltage to the bit line sensing amplifier after a predetermined delayed time from the bit line sensing start control signal.

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#### Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a power supply unit included in a conventional semiconductor memory device;

Fig. 2 is a circuit diagram showing a core voltage generator shown in Fig. 1;

Figs. 3A and 3B are circuit diagrams showing two different embodiments of an over driving controller shown in

Fig. 1;

Figs. 4A and 4B are circuit diagrams showing a bit line sensing amplifier shown in Fig. 1;

Fig. 5 is a circuit diagram showing a bit line sensing amplifier controller shown in Fig. 1;

Fig. 6 is a timing diagram showing variations of a core voltage at a normal operation of the conventional semiconductor memory device;

Fig. 7 is a timing diagram showing variations of a core voltage at a refresh operation of the conventional semiconductor memory device;

Fig. 8 is a block diagram showing a power supply unit included in a semiconductor memory device in accordance with the present invention;

Fig. 9 is a circuit diagram showing a bit line sensing start signal controller included in the power supply unit shown in Fig. 8;

Figs. 10A and 10B are circuit diagrams showing two different embodiments of an over driving controller shown in Fig. 8; and

Figs. 11 is a timing diagram showing variations of a core voltage at a refresh operation of the semiconductor memory device in accordance with the present invention.

## Detailed Description of Invention

Hereinafter, a power supply unit included in a

semiconductor memory device in accordance with the present invention will be described in detail referring to the accompanying drawings.

Fig. 8 is a block diagram showing the power supply unit  
5 included in the semiconductor memory device in accordance with the present invention.

As shown, the power supply unit includes a bit line sensing start signal controller 70, an over driving controller 71, a core voltage generator 72 and a bit line sensing  
10 amplifier 73.

The bit line sensing start signal controller 70 is controlled by a refresh signal REFB and a bit line sensing start signal SEST30 to generate a second bit line sensing start signal SEST30\_D.

15 The over driving controller 71 generates an over driving control signal SENSE\_EN for driving a power voltage VDD over a core voltage VCORE.

The core voltage generator 72 receives the over driving control signal SENSE\_EN, a reference voltage VRC and the  
20 second bit line sensing start signal SEST30\_D to generate the core voltage VCORE. If a voltage level of the core voltage VCORE downs and unstable when a bit line is charged, the core voltage generator 72 raises the core voltage VCORE to a stable voltage level. The core voltage generator 72 determines  
25 whether or not the core voltage VCORE is stable by comparing the core voltage VCORE with the reference voltage VRC.

The bit line sensing amplifier 73 amplifies data on a

bit line.

Although not shown in Fig. 8, there is also provided a bit line sensing amplifier controller for generating a first enable signal RTOE and a second enable signal SBE for  
5 supplying power to the bit line sensing amplifier 73.

Fig. 9 is a circuit diagram showing the bit line sensing start signal controller 70 shown in Fig. 8.

As shown, the bit line sensing start signal controller 70 includes a first block 61, a second block 62 and a  
10 selection unit 63. The bit line sensing start signal SEST30 is inputted through a first block 61 and a second block 62. The inputted bit line sensing start signal SEST30 is selected by the selection unit 63 to be outputted as the second bit line sensing start signal SEST30\_D.

15 If the semiconductor memory device is operated in a normal mode, the first block 61 is selected by the selection unit 63 to output the bit line sensing start signal SEST30 as the second bit line sensing start signal SEST30\_D through the first block 61. On the other hand, if the semiconductor  
20 memory device operates in a refresh mode, the second block 62 is selected by the selection unit 63 to output the bit line sensing start signal SEST30 as the second bit line sensing start signal SEST30\_D through the second block 62.

The second block 62 includes inverters I61 to I64 to  
25 delays the bit line sensing start signal SEST30.

The selection unit 63 is controlled by the refresh signal REFB to select the first and second blocks 61 and 62.

Therefore, the second bit line sensing start signal SEST30\_D is outputted from the first block 61 without delaying the bit line sensing start signal SEST30 in the normal mode; and, the SEST30\_D is outputted from the second block 62 after  
5 delaying the SEST30 for a predetermined time by the inverters I61 to I64 in the refresh mode.

Figs. 10A and 10B are circuit diagrams showing two different embodiments of the over driving controller 71. A first embodiment shown in Fig. 10A is provided with a  
10 plurality of inverters and a second embodiment shown in Fig. 10B is provided with a plurality of PMOS capacitors.

As described above, the over driving controller 71 generates the over driving control signal SENSE\_EN for driving the power voltage VDD over the core voltage VCore.

15 Referring to Fig. 10A, the over driving controller 71 includes inverters I81 to I87 and a NAND gate NAND81.

The inverters I31 to I37 invert and delay the bit line sensing start signal SEST30. The NAND gate NAND81 receives the bit line sensing start signal SEST30 and an outputted  
20 signal from the inverters I81 to I87, and performs NAND operation on the two received signals the bit line sensing start signal SEST30 and the outputted signal from the inverters I81 to I87.

Referring to Fig. 10B, the over driving controller 71  
25 includes inverters I88 to I93, a NAND gate NAND82, an NMOS transistor N81 and PMOS transistors P81 to P88.

Fig. 11 is a timing diagram showing variations of the



core voltage V<sub>CORE</sub> during the refresh operation of the semiconductor memory device in accordance with the present invention.

Referring to Figs. 8 to 11, operation of the present  
5 invention is described below.

As described above, the bit line sensing start signal SE<sub>ST30</sub> is outputted through the first block 61 or the second block 62 depending on the selection unit 63 controlled by the refresh signal RE<sub>FB</sub>.

10 In the normal mode, the refresh signal RE<sub>FB</sub> becomes a logic 'HIGH' level, whereby a transistor T<sub>1</sub> is turned on so that the bit line sensing start signal SE<sub>ST30</sub> can be outputted through the first block 61.

In the refresh mode, the refresh signal RE<sub>FB</sub> becomes a  
15 logic 'LOW' level, whereby a transistor T<sub>2</sub> is turned on so that the bit line sensing start signal SE<sub>ST30</sub> can be outputted through the second block 62.

Therefore, since the SE<sub>ST30</sub> is delayed in the second block 62, the timing for driving the power voltage V<sub>DD</sub> over  
20 the core voltage V<sub>CORE</sub> is also delayed in the refresh mode.

As shown in Fig. 11, the core voltage V<sub>CORE</sub> is stabilized during the refresh operation. Because excessive power consuming time of the core voltage V<sub>CORE</sub> is delayed for a predetermined time in the refresh mode than that in the  
25 normal mode, the core voltage V<sub>CORE</sub> can be stabilized since the timing for driving the power voltage V<sub>DD</sub> over the core voltage V<sub>CORE</sub> is also delayed for the predetermined time in

the refresh operation.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and  
5 modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.